NC7WZ86 TinyLogic® UHS Dual 2-Input Exclusive-OR Gate

General Description
The NC7WZ86 is a dual 2-Input Exclusive-OR Gate from Fairchild’s Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad VCC operating range. The device is specified to operate over the 1.65V to 5.5V VCC range. The inputs and output are high impedance when VCC is 0V. Inputs tolerate voltages up to 7V independent of VCC operating voltage.

Features
- Space saving USB surface mount package
- MicroPak™ Pb-Free leadless package
- Ultra High Speed; tPD 2.9 ns typ into 50 pF at 5V VCC
- High Output Drive; ±24 mA at 3V VCC
- Broad VCC Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Product Code Top Mark</th>
<th>Package Description</th>
<th>Supplied As</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC7WZ86K8X</td>
<td>MAB08A</td>
<td>WZ86</td>
<td>8-Lead USB, JEDEC MO-187, Variation CA 3.1mm Wide</td>
<td>3k Units on Tape and Reel</td>
</tr>
<tr>
<td>NC7WZ86LBX</td>
<td>MAC08A</td>
<td>N7</td>
<td>Pb-Free 8-Lead MicroPak, 1.6 mm Wide</td>
<td>5k Units on Tape and Reel</td>
</tr>
</tbody>
</table>

Logic Symbol

Connection Diagrams

Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Names</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN, BN</td>
<td>Input</td>
</tr>
<tr>
<td>YN</td>
<td>Output</td>
</tr>
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</table>

Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

H = HIGH Logic Level \ L = LOW Logic Level

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Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{CC}$) | $-0.5V$ to $+7V$
---|---
DC Input Voltage ($V_{IN}$) | $-0.5V$ to $+7V$
DC Output Voltage ($V_{OUT}$) | $-0.5V$ to $+7V$
DC Input Diode Current ($I_{IK}$)  @$V_{IN} < -0.5V$ | $-50mA$
DC Output Diode Current ($I_{OK}$)  @$V_{OUT} < -0.5V$ | $-50mA$
DC $V_{CC}$/GND Current ($I_{CC}/I_{GND}$) | $+100mA$
Storage Temperature ($T_{STG}$) | $-65°C$ to $+150°C$
Junction Temperature under Bias ($T_J$) | $150°C$
Junction Lead Temperature ($T_L$); (Soldering, 10 seconds) | $260°C$
Power Dissipation ($P_D$) @ $+85°C$ | $250mW$

Recommended Operating Conditions (Note 2)

Supply Voltage Operating ($V_{CC}$) | $1.65V$ to $5.5V$
Input Voltage ($V_{IN}$) | $0V$ to $5.5V$
Output Voltage ($V_{OUT}$) | $0V$ to $V_{CC}$
Operating Temperature ($T_A$) | $-40°C$ to $+85°C$
Input Rise and Fall Time ($t_R$, $t_F$)  
$V_{CC} = 1.8V$ | $±0.15V$, $2.5V$ to $±0.2V$; $0ns/V$ to $20ns/V$
$V_{CC} = 3.3V$ | $±0.3V$; $0ns/V$ to $10ns/V$
$V_{CC} = 5.0V$ | $±0.5V$; $0ns/V$ to $5ns/V$
Thermal Resistance ($\theta_{JA}$) | $250°C/W$

DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V_{CC}$</th>
<th>$T_A = +25°C$</th>
<th>$T_A = -40°C$ to $+85°C$</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
</table>
| $V_{IH}$ | HIGH Level Input Voltage | $1.65$ to $1.95$ | $0.75V_{CC}$ | $0.75V_{CC}$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -100\mu A$
| | | $2.3$ to $5.5$ | $0.7V_{CC}$ | $0.7V_{CC}$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -4mA$
| $V_{IL}$ | LOW Level Input Voltage | $1.65$ to $1.95$ | $0.25V_{CC}$ | $0.25V_{CC}$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -8mA$
| | | $2.3$ to $5.5$ | $0.3V_{CC}$ | $0.3V_{CC}$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -16mA$
| $V_{OH}$ | HIGH Level Output Voltage | $1.65$ | $1.55$ | $1.65$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -24mA$
| | | $2.3$ | $2.2$ | $2.3$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -32mA$
| | | $3.0$ | $2.9$ | $3.0$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -24mA$
| | | $4.5$ | $4.4$ | $4.5$ | $V$ | $V_{IN} = V_{IH}$, $V_{IL}$; $I_{CH} = -32mA$
| $V_{OL}$ | LOW Level Output Voltage | $1.65$ | $0.0$ | $0.1$ | $V$ | $V_{IN} = V_{IH}$ or $V_{IL}$; $I_{OL} = 100\mu A$
| | | $2.3$ | $0.0$ | $0.1$ | $V$ | $V_{IN} = V_{IH}$ or $V_{IL}$; $I_{OL} = 4mA$
| | | $3.0$ | $0.0$ | $0.1$ | $V$ | $V_{IN} = V_{IH}$ or $V_{IL}$; $I_{OL} = 8mA$
| | | $4.5$ | $0.0$ | $0.1$ | $V$ | $V_{IN} = V_{IH}$ or $V_{IL}$; $I_{OL} = 16mA$
| $I_{IN}$ | Input Leakage Current | $0$ to $5.5$ | $±0.1$ | $±1$ | $\mu A$ | $V_{IN} = 5.5V$, $GND$
| $I_{OFF}$ | Power Off Leakage Current | $0$ | $1$ | $10$ | $\mu A$ | $V_{IN}$ or $V_{OUT} = 5.5V$
| $I_{CC}$ | Quiescent Supply Current | $1.65$ to $5.5$ | $1$ | $10$ | $\mu A$ | $V_{IN} = 5.5V$, $GND$
### AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V_{CC}$ (V)</th>
<th>$T_A = -25^\circ C$</th>
<th>$T_A = -40^\circ C$ to $+85^\circ C$</th>
<th>Units</th>
<th>Conditions</th>
<th>Figure Number</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>CL = 15 pF, $R_L = 1 \text{ M}\Omega$</td>
</tr>
<tr>
<td>$t_{PLH}$, $t_{PHL}$ Propagation Delay</td>
<td>1.8 ± 0.15</td>
<td>2.0</td>
<td>6.7</td>
<td>12.5</td>
<td>2.0</td>
<td>13.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5 ± 0.2</td>
<td>1.2</td>
<td>4.1</td>
<td>7.0</td>
<td>1.2</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3 ± 0.3</td>
<td>0.5</td>
<td>2.2</td>
<td>3.5</td>
<td>0.5</td>
<td>3.8</td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$, $t_{PHL}$ Propagation Delay</td>
<td>3.3 ± 0.3</td>
<td>1.2</td>
<td>3.8</td>
<td>5.4</td>
<td>1.2</td>
<td>5.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.0 ± 0.5</td>
<td>0.8</td>
<td>2.9</td>
<td>4.2</td>
<td>1.0</td>
<td>4.6</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$ Input Capacitance</td>
<td>0</td>
<td>2.5</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{PD}$ Power Dissipation Capacitance</td>
<td>3.3</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

*Note 3: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. (See Figure 2.) $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC statically}).*

### AC Loading and Waveforms

**FIGURE 1. AC Test Circuit**

$C_c$ includes load and stray capacitance

Input PRR = 1.0 MHz; $t_r = 500$ ns

**FIGURE 2. $I_{CCD}$ Test Circuit**

Input = AC Waveform; $t_i = t_f = 1.8$ ns;

PRR = 10 MHz; Duty Cycle = 50%

**FIGURE 3. AC Waveforms**
# Tape and Reel Specification

## TAPE FORMAT for US8

<table>
<thead>
<tr>
<th>Package Designator</th>
<th>Tape Section</th>
<th>Number Cavities</th>
<th>Cavity Status</th>
<th>Cover Tape Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>K8X</td>
<td>Leader (Start End)</td>
<td>125 (typ)</td>
<td>Empty</td>
<td>Sealed</td>
</tr>
<tr>
<td></td>
<td>Carrier</td>
<td>3000</td>
<td>Filled</td>
<td>Sealed</td>
</tr>
<tr>
<td></td>
<td>Trailer (Hub End)</td>
<td>75 (typ)</td>
<td>Empty</td>
<td>Sealed</td>
</tr>
</tbody>
</table>

### TAPE DIMENSIONS inches (millimeters)

![Tape Dimensions Diagram](image)

## TAPE FORMAT for MicroPak

<table>
<thead>
<tr>
<th>Package Designator</th>
<th>Tape Section</th>
<th>Number Cavities</th>
<th>Cavity Status</th>
<th>Cover Tape Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>L8X</td>
<td>Leader (Start End)</td>
<td>125 (typ)</td>
<td>Empty</td>
<td>Sealed</td>
</tr>
<tr>
<td></td>
<td>Carrier</td>
<td>3000</td>
<td>Filled</td>
<td>Sealed</td>
</tr>
<tr>
<td></td>
<td>Trailer (Hub End)</td>
<td>75 (typ)</td>
<td>Empty</td>
<td>Sealed</td>
</tr>
</tbody>
</table>

### TAPE DIMENSIONS inches (millimeters)

![Tape Dimensions Diagram](image)
**Tape and Reel Specification** (Continued)

**REEL DIMENSIONS** inches (millimeters)

<table>
<thead>
<tr>
<th>Tape Size</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>N</th>
<th>W1</th>
<th>W2</th>
<th>W3</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>7.0</td>
<td>0.059</td>
<td>0.512</td>
<td>0.795</td>
<td>2.165</td>
<td>0.331 + 0.059/–0.000</td>
<td>0.567</td>
<td>W1 + 0.078/–0.039</td>
</tr>
<tr>
<td></td>
<td>(177.8)</td>
<td>(1.50)</td>
<td>(13.00)</td>
<td>(20.20)</td>
<td>(55.00)</td>
<td>(8.40 + 1.50/–0.00)</td>
<td>(14.40)</td>
<td>(W1 + 2.00/–1.00)</td>
</tr>
</tbody>
</table>
Physical Dimensions

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTENSIONS.
Physical Dimensions  inches (millimeters) unless otherwise noted (Continued)

![Physical Dimensions Diagram]

Notes:
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14M-1994
4/  PIN 1 FLAG, END OF PACKAGE OFFSET.

Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

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